VLIW COMPUTER PROCESSING ARCHITECTURE WITH ON-CHIP DRAM USABLE AS PHYSICAL MEMORY OR CACHE MEMORY

ABSTRACT OF THE DISCLOSURE

According to the invention, a first processor chip (10) comprising a processing core (12) and at least one bank of memory(14). The at least one bank of memory (14) preferably includes a mode control input (32) for controlling the mode of the at least one bank of memory (14) between physical memory and cache memory. In addition, the first processor chip (10) may further comprise an I/O link (26) configured to facilitate communication between the first processor chip (10) and other processor chips, and a communication and memory controller (20, 22) in electrical communication with the processing core (12), the at least one bank of memory (14), and the I/O link (26). The communication and memory controller (20, 22) preferably controls the exchange of data between the first processor chip (10) and the other processor chips, as well as receive memory requests from the processing core (12) of the first processor chip (10) and from other processing cores residing on the other processor chips, and process the memory requests with the at least one bank of memory (14). The memory requests from the other processing cores on the other processor chips preferably are received by the first processor chip (10) through the I/O link (26).

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